AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor device provided with a semiconductor substrate; a gate electrode formed on said semiconductor substrate; and an impurity diffusion region formed beside said gate electrode with a PN junction with a region in the semiconductor substrate; wherein:

the impurity diffusion region comprises a first impurity diffusion region including a first P-type impurity and located in the proximity of a surface of the semiconductor substrate; and

a second P-type impurity diffusion region located below the first impurity diffusion region and including a second P-type impurity having a smaller diffusion coefficient in the semiconductor substrate than the first P-type impurity, each of said first impurity diffusion region and said second impurity diffusion region forming the PN junction with the region of the semiconductor substrate.

2. (original): The semiconductor device in accordance with the Claim 1, wherein a concentration of the second P-type impurity in the second impurity diffusion region is lower than a concentration of the first P-type impurity in the first impurity diffusion region.

3. (original): The semiconductor device in accordance with the Claim 1, wherein the first P-type impurity includes B.

4. (original): The semiconductor device in accordance with the Claim 1, wherein the second P-type impurity includes In.

5. (original): The semiconductor device in accordance with the Claim 1, wherein said impurity diffusion regions are provided on both sides of said gate electrode.

6. (withdrawn): A method of manufacturing a semiconductor device provided with a semiconductor substrate, a gate electrode formed on said semiconductor substrate and an impurity diffusion region formed beside said gate electrode, comprising:

forming a first impurity diffusion region that constitutes a part of said impurity diffusion region by ion implantation of the first P-type impurity in a region beside said gate electrode in the proximity of a surface of said semiconductor substrate; and

forming a second impurity diffusion region that constitutes a part of said impurity diffusion region by ion implantation of a second P-type impurity having a smaller diffusion coefficient in said semiconductor substrate than the first P-type impurity, in a region below the first impurity diffusion region.

7. (withdrawn): The method in accordance with the Claim 6,

wherein the step of forming the second impurity diffusion region includes executing ion implantation of the second P-type impurity in the second impurity diffusion region, such that a lower concentration is achieved than a concentration of the first P-type impurity implanted in the first impurity diffusion region.

8. (withdrawn): The method in accordance with the Claim 6, wherein the step of forming the first impurity diffusion region includes executing ion implantation of B as the first P-type impurity.

9. (withdrawn): The method in accordance with the Claim 6, wherein the step of forming the second impurity diffusion region includes executing ion implantation of In as the second P-type impurity.

10. (withdrawn): The method in accordance with the Claim 9, wherein the step of forming the second impurity diffusion region includes executing ion implantation of the second P-type impurity with an implanting energy of not less than 80 keV but not greater than 180 keV.

11. (withdrawn): The method in accordance with the Claim 9,

wherein the step of forming the second impurity diffusion region includes executing ion implantation of the second P-type impurity in an implanting amount of not less than 5x1012 cm-2 but not greater than 1.5x1013 cm-2.

12. (withdrawn): The method in accordance with the Claim 6, wherein the step of forming the first impurity diffusion region is carried out after the step of forming the second impurity diffusion region.

13. (withdrawn): The method in accordance with the Claim 6, further comprising:

activating the first P-type impurity and the second P-type impurity by heat treatment of the first impurity diffusion region and the second impurity diffusion region.

14. (new): A semiconductor device provided with a semiconductor substrate;

a pair of LDD regions formed apart from each other to define a channel region;

a gate electrode formed over the channel region,

a source region formed in contact with one of the LDD regions on an opposite side of the channel region; and

a drain region formed in contact with another LDD region on an opposite side of the channel region;

each of said source region and said drain region comprises a first impurity diffusion region including a first P-type impurity and located in the proximity of a surface of the semiconductor substrate;

a second P-type impurity diffusion region located below the first impurity diffusion region and including a second P-type impurity having a smaller diffusion coefficient in the semiconductor substrate than the first P-type impurity; and

each of the LDD regions including the first P-type impurity and not including the second P-type impurity.

15. (new): A semiconductor device according to claim 14, wherein a concentration of the second P-type impurity in the second impurity diffusion region is lower than a concentration of the first P-type impurity in the first impurity diffusion region.

16. (new): A semiconductor device according to claim 14, wherein the first P-type impurity includes B.

17. (new): A semiconductor device according to claim 14, wherein the second P-type impurity includes In.

18. (new): A semiconductor device, comprising:

a gate electrode formed on a semiconductor substrate;

a LDD region formed beside said gate electrode, the LDD region including a first P-type impurity;

a sidewall formed on a lateral face of said gate electrode;

a first impurity diffusion region formed beside the sidewall and in deeper position than the LDD region, the first impurity diffusion region including the first P-type impurity;

a second impurity diffusion region that is formed beside the sidewall and in further deeper position than the first impurity diffusion region, said second impurity diffusion region including a second P-type impurity that has a smaller diffusion coefficient than a first P-type impurity, wherein an impurity concentration of the second impurity diffusion region is lower than that of the first impurity diffusion region, and distance between second impurity diffusion regions that are formed on both sides of the gate electrode is larger than that between first impurity diffusion regions that are formed on both sides of the gate electrode.

19. (new): A semiconductor device according to claim 18, wherein the first P-type impurity includes B.

20. (new): A semiconductor device according to claim 18, wherein the second P-type impurity includes In.

21. (new) : A semiconductor device according to claim 18, wherein the impurity concentration of said first impurity diffusion region has a steeper gradient in a depth wise direction than that of second impurity diffusion region.